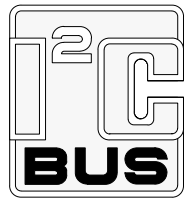
DATA SHEET



PCA9558

8-bit I^2C and SMBus I/O port with 5-bit multiplexed/1-bit latched 6-bit I^2C EEPROM DIP switch and 2-kbit EEPROM

Product data
Supersedes data of 2002 May 24

2003 Jun 27

Philips Semiconductors

PHILIPS

8-bit I²C and SMBus I/O port with 5-bit multiplexed/1-bit latched 6-bit I²C EEPROM DIP switch and 2-kbit EEPROM

PCA9558

FEATURES

- 5-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 6-bit MUX_OUTx and NON_MUXED_OUT EEPROM programmable and readable via I²C-bus
- 5 V tolerant open drain MUX_OUTx and NON_MUXED_OUT outputs
- Active-LOW override input forces all MUX_OUTx outputs to logic 0
- I²C readable MUX_INx inputs
- 5 V tolerant open drain I/Ox pins, power-up default as outputs
- 1 address pin, allowing up to 2 devices on the I²C-bus
- Active-LOW reset input with internal pull-up for the 8 I/O pins
- 2048-bit EEPROM programmable and readable via the I²C or I/Os
- Operating power supply voltage range of 3.0 V to 3.6 V
- SMBus compliance with fixed 3.3 V levels
- 2.5 V to 5 V tolerant inputs
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

The PCA9558 is a highly integrated, multi-function device that is composed of a 5-bit multiplexed/1-bit latched 6-bit I²C/SMBus EEPROM DIP switch, an 8-bit I/O expander and a 2-kbit serial EEPROM with write protect. The PCA9558 integrates these commonly used components into a single chip to reduce component count and board space requirements and is useful in computer, server and telecom/networking applications.

Multiplexed/latched EEPROM DIP switch — used to select digital information between a set of 5-bits of default hardware inputs and an alternative set of inputs provided by the I²C/SMBus interface and stored in the EEPROM. Examples of this type of selection include processor voltage configuration or processor vendor identification (VID). The multiplexed/latched EEPROM can also be used to replace DIP switches or jumpers, since the settings can be easily changed via I²C/SMBus without having to power down the equipment to open the cabinet. The non-volatile memory retains the most current setting selected before the power is turned off.

8-bit I/O expander — used to control, monitor or collect remote information or power LEDs. Monitored or collected information can be read through the I²C/SMBus or can be stored in the internal EEPROM.

2-kbit serial EEPROM — used to store information such as card identification or revision/maintenance history on every motherboard/linecard and can be read or written via I²C/SMBus when required.

The PCA9558 has 1 address pin allowing up to 2 devices to be placed on the same I²C-bus or SMBus.

PIN CONFIGURATION

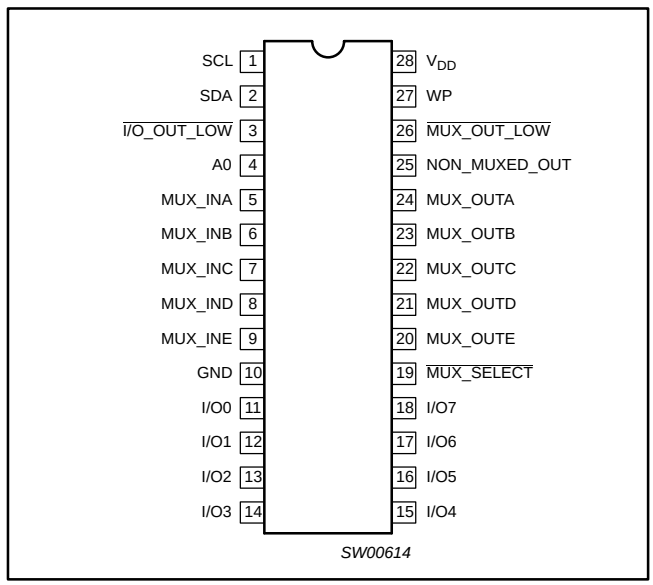


Figure 1. Pin configuration

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
28-Pin Plastic TSSOP	0 to +70 °C	PCA9558PW	PCA9558DH	SOT361-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	SCL	Serial I²C-bus clock
2	SDA	Serial bi-directional I²C-bus data
3	$\overline{\text{I/O\_OUT\_LOW}}$	Active-LOW control forces all GPIO to logic 0 outputs
4	A0	A0 Address
5-9	MUX_IN A-E	External inputs to multiplexer
10	GND	Ground
11-18	I/O[0-7]	General purpose Input/Output 0 through 7 (open drain outputs)
19	$\overline{\text{MUX\_SELECT}}$	Active-LOW Select of MUX_IN inputs or EEPROM contents for MUX_OUT outputs
20-24	MUX_OUT E-A	Open drain multiplexed outputs
25	NON_MUXED_OUT	Open drain outputs from non-volatile memory
26	$\overline{\text{MUX\_OUT\_LOW}}$	Active-LOW control forces all MUX outputs to logic 0
27	WP	Active-HIGH EEPROM write protect
28	V_{DD}	Power supply : +3.0 to +3.6 V

BLOCK DIAGRAM

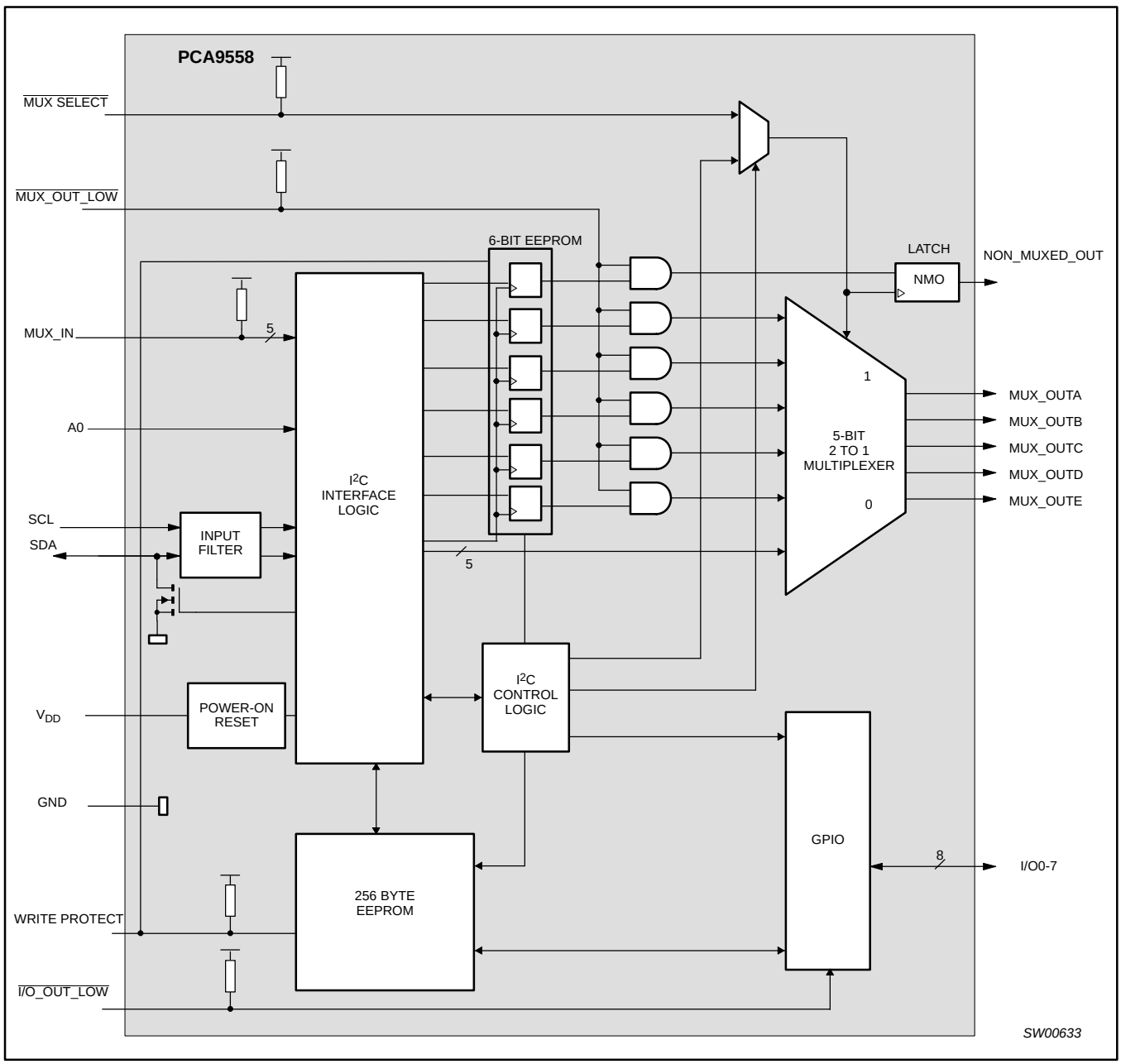


Figure 2. Block diagram

I²C INTERFACE

Communicating with this device is initiated by sending a valid address on the I²C-bus. The address format (see FIgure 3) has 6 fixed bits and one user-programmable bits followed by a 1-bit read/write value which determines the direction of the data transfer.

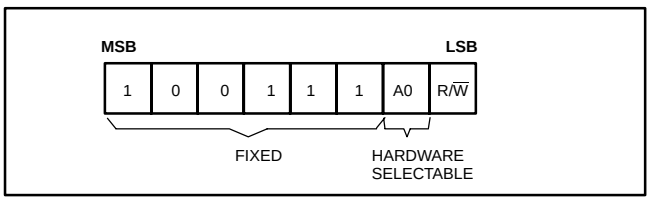


Figure 3. I²C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the EEPROM. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The four high-order bits are latched outputs, while the four low order bits are multiplexed outputs (Figure 5).

NOTE:

1. To ensure data integrity, the EEPROM must be internally write protected when V_{CC} to the I²C-bus is powered down or V_{CC} to the component is dropped below normal operating levels.

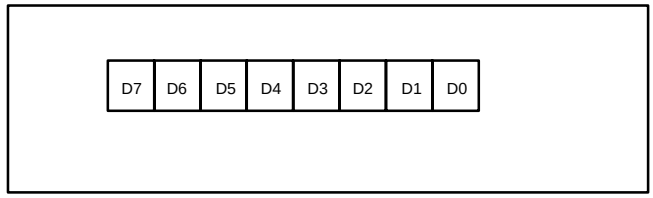


Figure 4. Command Byte

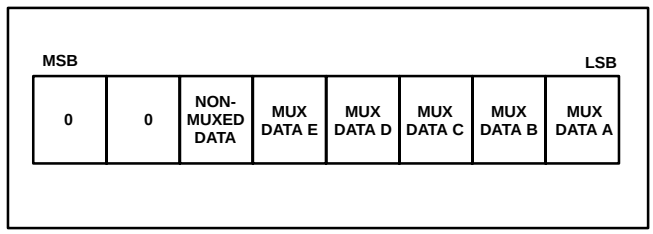


Figure 5. I²C MUX_OUT Data Byte

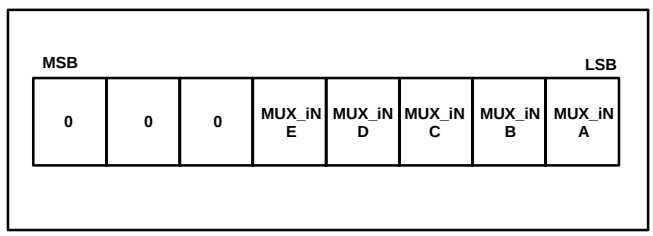


Figure 6. I²C MUX_IN Data Byte

Table 1. Command byte

D7	D6	D5	D4	D3	D2	D1	D0	COMMAND
0	0	0	0	0	0	0	1	Write to 256EE via I²C
0	0	0	0	0	0	1	1	Read from 256EE via I²C
0	0	0	0	0	1	0	0	Write to 6 bit EE via I²C
0	0	0	0	0	1	1	0	Read from 6 bit EE via I²C
0	0	0	0	0	1	1	1	Read IP (Input Port) Register via I²C
0	0	0	0	1	0	0	0	Read/Write OP (Outut Port) Register via I²C
0	0	0	0	1	0	0	1	Read/Write PI (Polarity Inversion) Register via I²C
0	0	0	0	1	0	1	0	Read/Write IOC (Input/Ouput Configuration) Register via I²C
0	0	0	0	1	0	1	1	Read/Write MUXCNTRL (Mux Control) Register via I²C
0	0	0	0	1	1	0	0	Read MUXIN values via I²C
0	0	0	0	1	1	0	1	Reserved
0	0	0	0	1	1	1	0	Reserved
0	0	0	0	1	1	1	1	Read 256EE and Write OP Register
0	0	0	1	0	0	0	0	Read 256EE and Write PI Register
0	0	0	1	0	0	0	1	Read 256EE and Write IOC Register
0	0	0	1	0	0	1	0	Read IP Register and Write to 256EE
0	0	0	1	0	0	1	1	Reserved
…	…	…	…	…	…	…	…	
1	1	1	1	1	1	1	1	Reserved

The Multiplexer function controls the six open drain outputs, MUX_OUTx and NON_MUXED_OUT. This control is effected by the input pins MUX_SELECT (Pin 19), $\overline{\text{MUX\_OUT\_LOW}}$ (Pin 26), and/or an internal register programmed via the I²C-bus. Upon power-up the multiplex function is controlled by the MUX_SELECT and $\overline{\text{MUX\_OUT\_LOW}}$ pins. When the MUX_SELECT signal is a logic 0, the multiplexer will select the data from the 6-bit EEPROM to drive on the MUX_OUTx and NON_MUXED_OUT pins. When the MUX_SELECT signal is a logic 1, the multiplexer will select the MUX_INx pins to drive on the MUX_OUTx pins. The NON_MUXED_OUT output is latched from the 6-bit EEPROM on a rising edge of the MUX_SELECT signal. This latch is transparent while the MUX_SELECT signal is a logic 0. An internal control register, written via the I²C-bus, can also control the multiplexer function. When this register is written, the MUX_SELECT function can change from the external pin to an internal register. In this register a bit will act in a similar fashion to the MUX_SELECT input, i.e., a logic 1 will cause the multiplexer to select data from the 6-bit EEPROM to drive on the MUX_OUTx and NON_MUXED_OUT pins. In this configuration, the NON_MUXED_OUT will latch data when the PCA9558 acknowledges the I²C-bus. The MUX_SELECT pin will have no effect on the MUX_OUTx or NON_MUXED_OUT while in this mode. When the $\overline{\text{MUX\_OUT\_LOW}}$ signal is a logic 0 and the multiplexer is configured so that the MUX_OUTx pins are being driven by the 6-bit EEPROM, the MUX_OUTx pins will be driven to a logic 0. This information is summarized in Table 2.

Table 2. Multiplexer function table

REG.		INPUT		OUTPUT	
B1[3]	B0[3]	MUX_OUT_LOW	MUX_SELECT	MUX_OUTx	NON_MUXED_OUT
x	0	0	1	MUX_INx inputs	latched from EEPROM[1]
x	0	0	0	0	0
x	0	1	1	MUX_INx inputs	latched from EEPROM[1]
x	0	1	0	from EEPROM	from EEPROM
0	1	0	x	MUX_INx inputs	latched from EEPROM[2]
1	1	0	x	0	0
0	1	1	x	MUX_INx inputs	latched from EEPROM[2]
1	1	1	x	from EEPROM	from EEPROM

NOTES:
1. NON_MUXED_OUT value will be the value present in the 6-bit EEPROM at the time of the rising edge of the MUX_SELECT input.
2. NON_MUXED_OUT value will be the value present int he 6-bit EEPROM at the time of the slave ACK when bit 1 has changed from '0' to '1'.
3. These are the 2 LSBs of the MUXCNTRL (Mux Control) Register

If the MUX_OUTx outputs are being driven by the 6-bit EEPROM and this EEPROM is programmed, the outputs will remain stable and change to the new values after the EEPROM program cycle completes.

Examples of Read/Write for MUX control can be found in Figure 7.

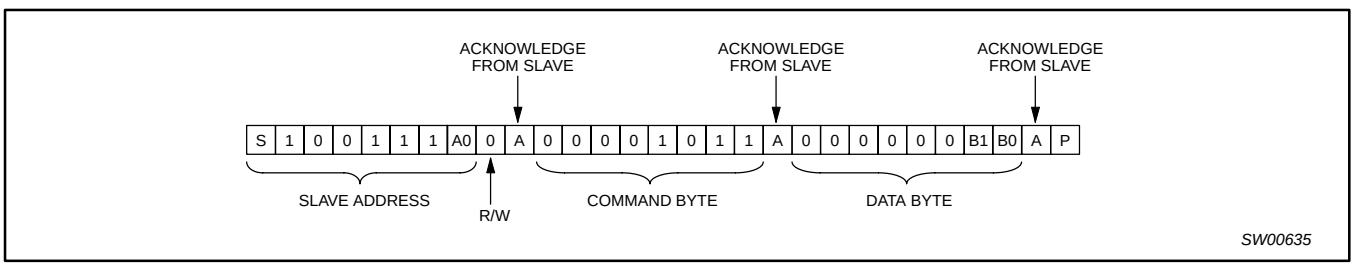


Figure 7. I²C write for MUXCNTRL register

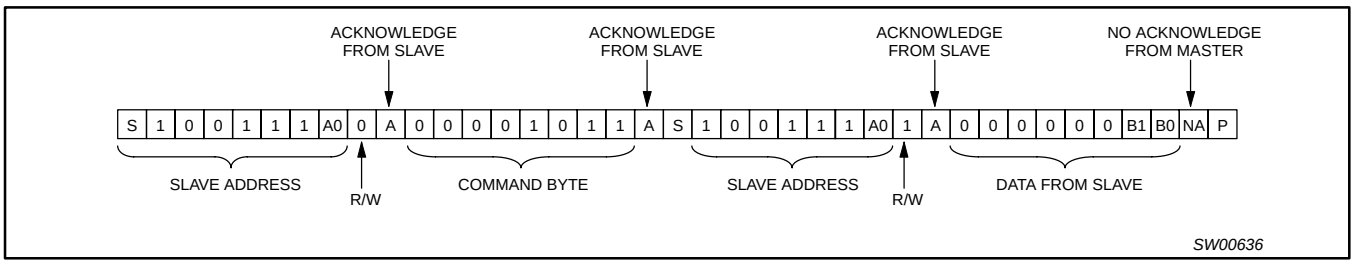


Figure 8. I²C read for MUXCNTRL register

The GPIOs are controlled by a set of 4 internal registers: Input Port Register (IPR); Output Port Register (OPR); Polarity Inversion Register (PIR); and the Input/Output Configuration Register (IOCR). Each register is read/write via the I²C-bus or 256 byte EEPROM, with the exception of the IPR, which is read only, one at a time. The read/write takes place on the slave ACKNOWLEDGE. The control of which register is currently available to the I²C-bus is set by bits in the control register. See Tables 3 through 6 for details.

Table 3. Input Port Register (IPR)

Bit	I7	I6	I5	I4	I3	I2	I1	I0
Default	0	0	0	0	0	0	0	0

This register is an input-only port. It reflects the logic value present on the GPIO pins regardless of whether they are configured as inputs or outputs (IOCR). Writes to this register have no effect.

Table 4. Output Port Register (OPR)

Bit	O7	O6	O5	O4	O3	O2	O1	O0
Default	0	0	0	0	0	0	0	0

This register is an output-only port. It reflects the outgoing logic levels of the GPIO defined as outputs in the IOCR. Bit values in this register have no effect on GPIO defined as inputs. In turn, reads from this register reflect the value stored in the flip-flop controlling the output, **not** the actual output value.

Table 5. Polarity Inversion Register (PIR)

Bit	P7	P6	P5	P4	P3	P2	P1	P0
Default	1	1	1	1	0	0	0	0

This register enables polarity inversion of GPIO defined as inputs by the IOCR. If a bit in this register is set to a logic 1, the corresponding GPIO input port is inverted. If a bit in this register is set to a logic 0, the corresponding GPIO input port is not inverted.

Table 6. I/O Configuration Register (IOCR)

Bit	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

This register configures the direction of the GPIO pins. If a bit is set to a logic 1, the corresponding port pin is enabled as an input with a high impedance output driver. If a bit is set to a logic 0, the corresponding port pin is enabled as an output.

Examples of Read/Write to these registers can be found in Figures 9, 10, 15, and 16.

The $\overline{\text{I/O\_OUT\_LOW}}$ input, when held LOW longer than the time t_W, will reset the GPIO registers to their default (power-up) values.

A read of the present value of the inputs MUX_INx can be done via the I²C. This is done by addressing the PCA9558 in a write mode and entering the correct command code. The preset value on the MUX_INx inputs is latched at the command code ACKNOWLEDGE. A REPEATED START is then sent with the R/$\overline{W}$ bit set to a logic 1, read, and this latched data is read out on the I²C-bus. See Figure 11.

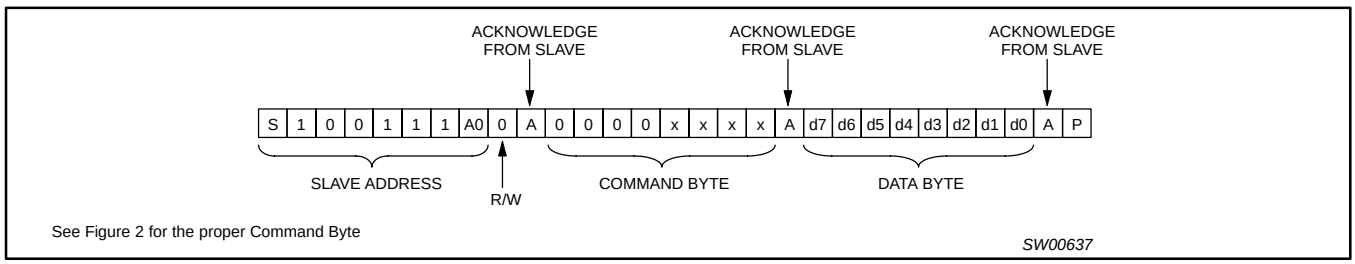


Figure 9. I2C write for GPIO registers

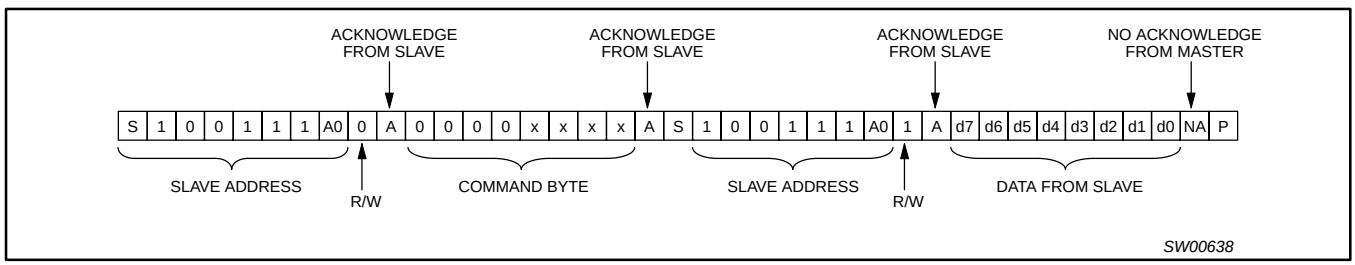


Figure 10. I2C read for GPIO registers

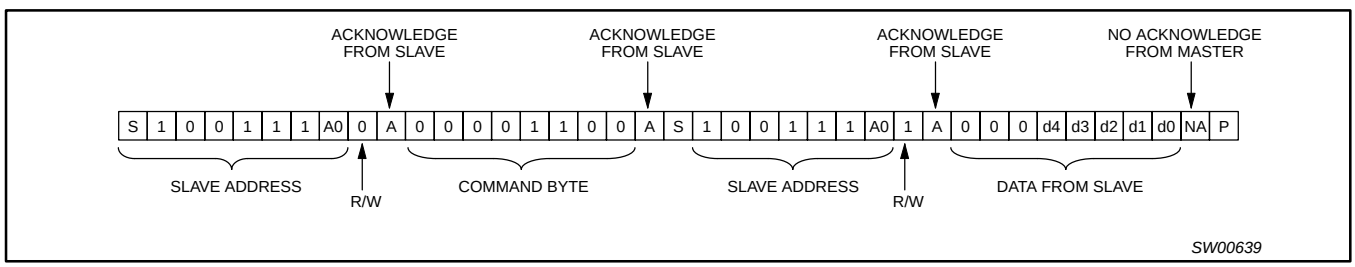


Figure 11. I2C read of MUX_INx inputs

EEPROM write operation

6-bit write operation
A write operation to the 6-bit EEPROM requires that an address byte be written after the command byte. This address points to the 6-bit address space in the EEPROM array. Upon receipt of this address, the PCA9558 waits for the next byte that will be written to the EEPROM. The master then ends the transaction with a STOP condition on the I²C. See Figure 12.

After the STOP condition, the E/W cycle starts, and the parts will not respond to any request to access the EEPROM array until the cycle finishes, approximately 4 ms.

6-bit read operation
A read operation is initiated in the same manner as a write operation, with the exception that after the word address has been written a REPEATED START condition is placed on the I²C-bus and the direction of communication is reversed (see Figure 13).

256 byte write operation (I²C)
A write operation to the 256 byte EEPROM requires that an address byte be written after the command byte. This address points to the starting address in the EEPROM array. The four LSBs of this address select a position on a 16 byte page register, the 4 MSBs select which page register. The four LSBs will be auto-incremented after receipt of each byte of data; in this manner, the entire page register can be written starting at any point. Up to 16 bytes of data may be sent to the PCA9558, followed by a STOP condition on the I²C-bus. If the master sends more than 16 bytes of data prior to generating a STOP condition, data within the address page will be overwritten and unpredictable results may occur. See Figure 14.

After the STOP condition, the E/W cycle starts, and the parts will not respond to any request to access the EEPROM array until the cycle finishes, approximately 4 ms.

256 byte read operation (I²C)
A read operation is initiated in the same manner as a write operation, with the exception that after the word address has been written, a REPEATED START condition is placed on the I²C-bus, and the direction of communication is reversed. For a read operation, the entire address is incremented after the transmission of each byte, meaning that the entire 256 byte EEPROM array can be read at one time. See Figure 15.

256 byte EEPROM write to GPIO
A mode is available whereby a byte of data in the 256 byte EEPROM array can be written to the GPIO (OPR). This is initiated by the I²C-bus. In this mode, a control word indicating a read from the 256 byte EEPROM and write to the GPIO is sent, followed by the word address of the data within the EEPROM array. Upon ACKNOWLEDGE from the slave, the data is sent to the GPIO. See Figure 16.

256 byte EEPROM write from GPIO
A mode is available whereby data in the GPIO (IPR) can be written to the 256 byte EEPROM. This is initiated by the I²C-bus. In this mode, a control word indicating a read from the GPIO and write to the 256 byte EEPROM is sent, followed by the word address for the data to be written. Once the slave sent an ACKNOWLEDGE, the master must send a STOP condition. See Figure 17.

After the STOP condition, the E/W cycle starts, and the parts will not respond to any request to access the EEPROM array until the cycle finishes, approximately 4 ms.

When the Write Protect (WP) input is a logic 0 it allows writes to both EEPROM arrays. When a logic 1, it prevents any writes to the EEPROM arrays.

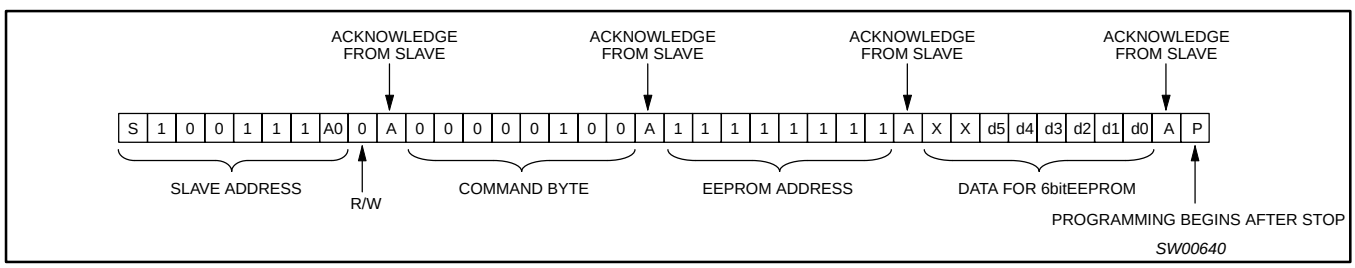


Figure 12. I²C write of 6-bit EEPROM

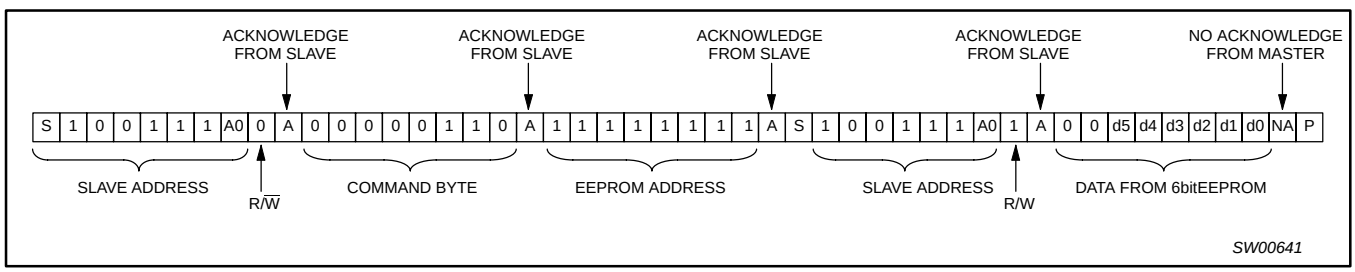


Figure 13. I²C read of 6-bit EEPROM

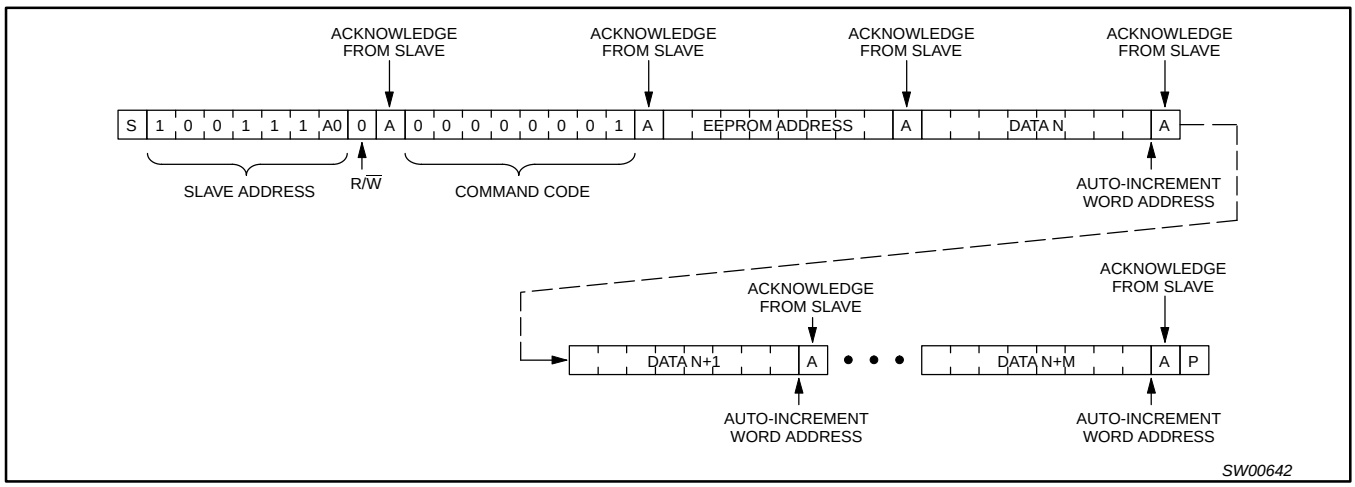


Figure 14. I²C page write operation to 256 byte EEPROM; M bytes where M ≤ 15

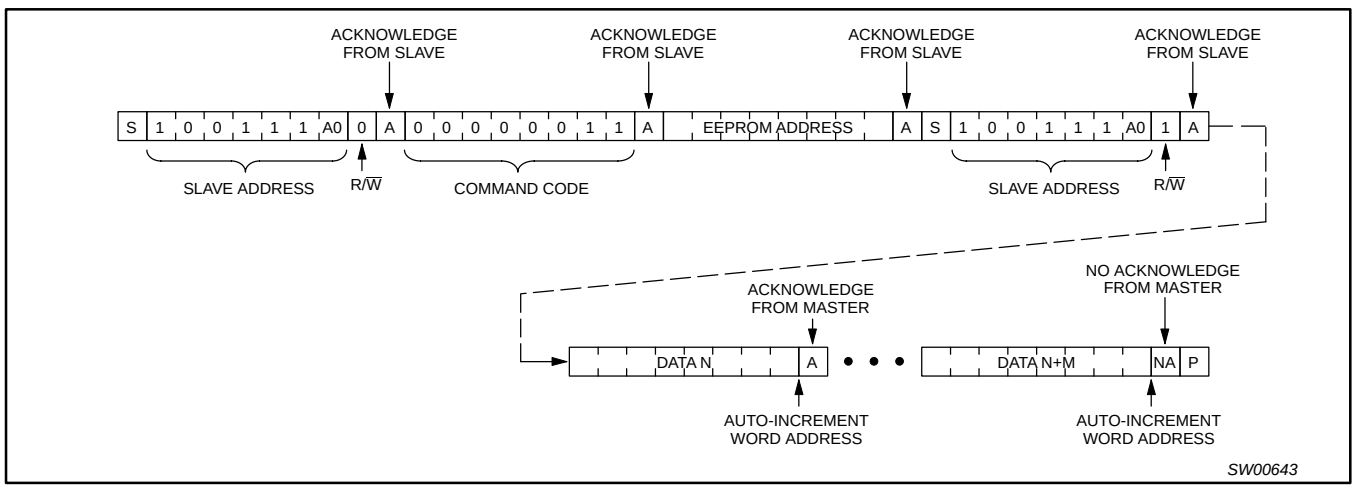


Figure 15. I²C read operation from 256 byte EEPROM; M bytes where M ≥ 1

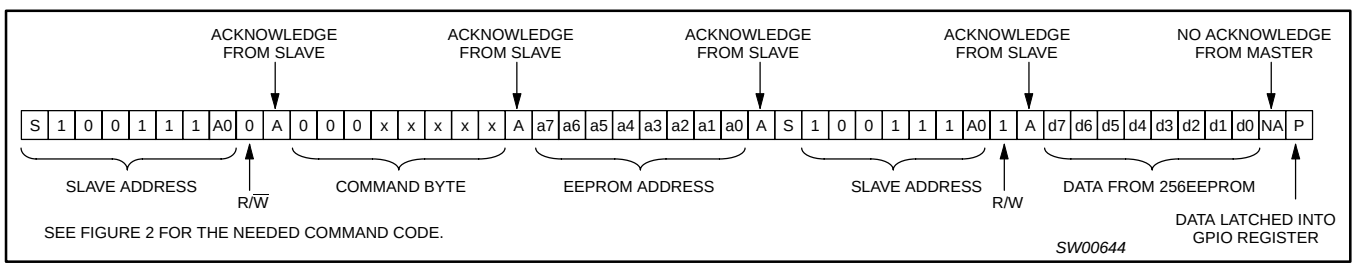


Figure 16. Read from 256 byte EEPROM and write to GPIO registers

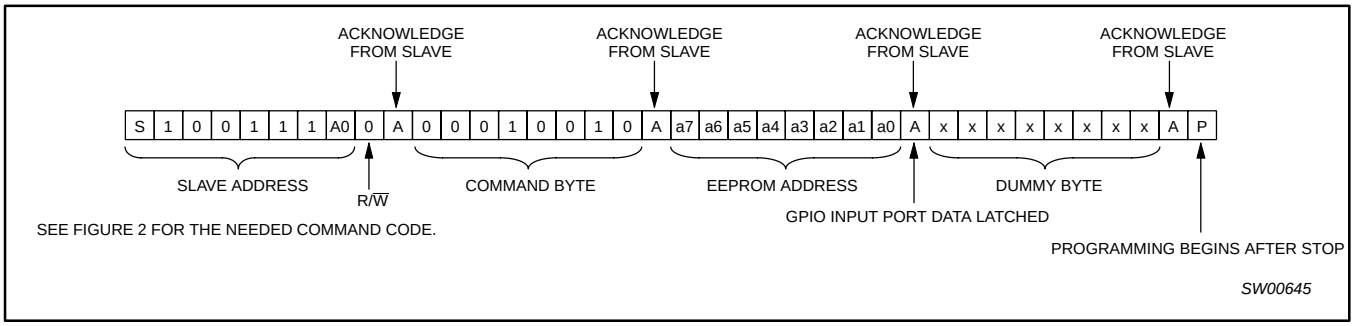


Figure 17. Read from GPIO Input Port Register and write to 256 byte EEPROM

RESET

Power-on Reset (POR)

When power is applied to V_{DD}, an internal power-on reset holds the PCA9558 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9558 volatile registers and SMBus state machine will initialize to their default states.

The GPIO outputs will be selected as inputs and in high impedance. The DIP Switch MUX_OUT and NON_MUXED_OUT pin values depend on:

- the MUX_OUT_LOW and MUX_SELECT logic levels
- the previously stored values in the EEPROM register/current MUX_IN pin values as shown in Table 2.

External Reset

A reset of the GPIO registers can be accomplished by holding the $\overline{\text{I/O\_OUT\_LOW}}$ pin LOW for a minimum of tw. These GPIO registers return to their default states until the $\overline{\text{I/O\_OUT\_LOW}}$ input is once again HIGH.

USING THE PCA9558 ON THE SMBus

It is possible to use Intel® chipsets to communicate with the PCA9558. There are no limitations when the SMBus Controller is communicating with the Mux or the GPIO; however, there are limitations with the 2K serial EEPROM. Because of being able to address any location in the EEPROM block using the 2nd command byte, the designer using the PCA9558 on the SMBus will have to program around it, an easy thing to do. The device designers had to deal with the specifics of addressing the EEPROM and chose the I²C spec and use the 2nd command byte to address any location in the EEPROM block.

In order to write to the EEPROM, write the EEPROM address byte in the Data0 byte and the data to be sent should be placed in the Data1 byte. The Intel® chipset's Word Data instruction would then send the address, followed by the command register then Data0 (EEPROM address), and then the Data1 (data byte). A read from the EEPROM would be a two step process. The first step would be to do a Write Byte with the EEPROM address in the Data0 register. The second step would be to do a Receive Byte where the data is stored in the command register.

Other differences from the SMBus spec:

Paragraph 5.5.5 - Read Byte/Word in figure 5-11 - the PCA9558 follows this same command code with one exception, the PCA9558 requires 2 bytes of command before the repeated start.

Paragraph 5.5.6 - Process call in figure 5-15 - the PCA9558 read operation is very similar to the SMBus process call. In the PCA9558 read operation you send a start condition - slave address with a write bit - 2 bytes of command code - repeated start - slave address with a read bit - then read data.

® Intel is a registered trademark of Intel Corporation.

TYPICAL APPLICATION

Applications

- Board version tracking and configuration
- Board health monitoring and status reporting
- Multi-card systems in Telecom, Networking and Base Station Infrastructure Equipment
- Field recall and troubleshooting functions for installed boards
- General-purpose integrated I/O with DIP switch and memory

A central processor/controller typically located on the system main board can use the 400 kHz I²C/SMBus to poll the PCA9558 devices located on the system cards for status or version control type of information. The PCA9558 may be programmed at manufacturing to store information regarding board build, firmware version, manufacturer identification, configuration option data… Alternately, these devices can be used as convenient interface for board configuration, thereby utilizing the I²C/SMBus as an intra-system communication bus.

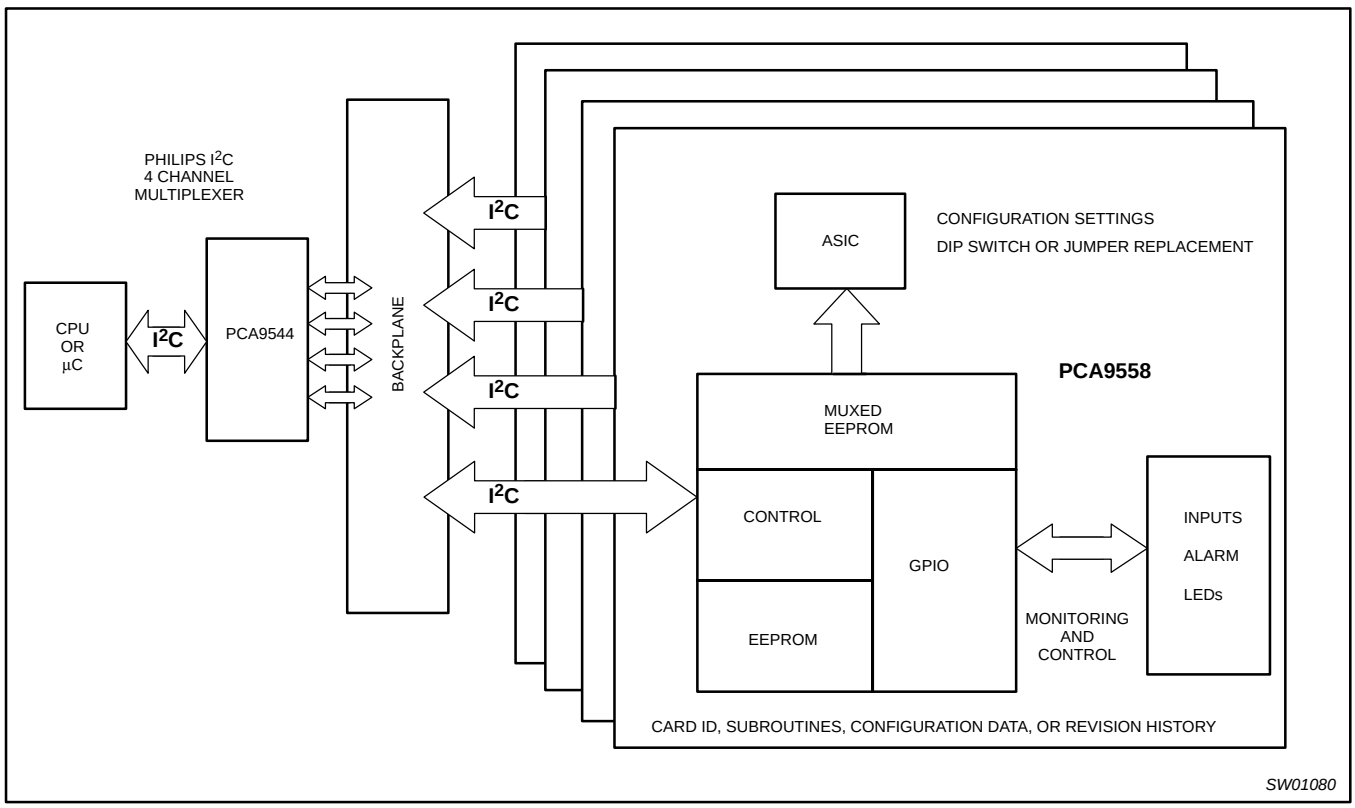


Figure 18. Typical application

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	DC supply voltage		2.5 to 4.6	V
V_I	DC input voltage	Note 3	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC output voltage	Note 3	-0.5 to V_{CC} +0.5	V
T_{stg}	Storage temperature range		-60 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		CONDITIONS	LIMITS		UNIT
				MIN	MAX	
V_{DD}	DC supply voltage			3	3.6	V
V_{IL}	LOW-level input voltage	SCL, SDA	I_{OL}= 3 mA	-0.5	0.9	V
V_{IH}	HIGH-level input voltage	SCL, SDA	I_{OL}= 3 mA	2.7	4.0	V
V_{OL}	LOW-level output voltage	SCL, SDA	I_{OL}= 3 mA	—	0.4	V
			I_{OL}= 6 mA	—	0.6	V
V_{IL}	LOW-level input voltage	$\overline{\text{MUX\_OUT\_LOW}}$, MUX_IN, MUX_SELECT		-0.5	0.8	V
V_{IH}	HIGH-level input voltage	$\overline{\text{MUX\_OUT\_LOW}}$, MUX_IN, MUX_SELECT		2.0	4.0	V
I_{OL}	LOW-level output current	MUX_OUT, NON_MUXED_OUT	V_{OL} = 0.4 V	—	4	mA
I_{OH}	HIGH-level output current	MUX_OUT, NON_MUXED_OUT		—	100	µA
dt/dv	Input transition rise or fall time			0	10	ns/V
T_{amb}	Operating temperature			0	+70	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supply						
V_{DD}	Supply voltage		3.0	—	3.6	V
I_{CCL}	Supply current	Operating mode ALL inputs = 0 V	—	—	10	mA
I_{CCH}	Supply current	Operating mode ALL inputs = V_{DD}	—	—	10	mA
V_{POR}	Power-on reset voltage	no load; $V_I = V_{DD}$ or GND	—	2.3	2.6	V
Input SCL: Input/Output SDA						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2	—	V_{CC} + 0.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
I_{OL}	LOW-level output current	V_{OL} = 0.6 V	6	—	—	mA
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	-1	—	1	µA
I_{IL}	Leakage current LOW	V_I = GND	-1	—	1	µA
C_I	Input capacitance		—	—	10	pF
$\overline{\text{MUX\_OUT\_LOW}}$, WP, MUX_SELECT						
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	—	—	1	µA
I_{IL}	Leakage current LOW	V_I = GND	—	—	-100	µA
C_I	Input capacitance		—	—	10	pF
MUX_IN A → MUX_IN E						
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	—	—	1	µA
I_{IL}	Leakage current LOW	V_I = GND	—	—	-100	µA
C_I	Input capacitance		—	—	10	pF
A0 Inputs						
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	—	—	1	µA
I_{IL}	Leakage current LOW	V_I = GND	—	—	-100	µA
C_I	Input capacitance		—	—	10	pF
MUX_OUTx						
V_{OL}	LOW-level output current	I_{OL} = 100 µA	—	—	0.4	V
V_{OL}	LOW-level output current	I_{OL} = 4 mA	—	—	0.7	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$	—	—	100	µA
NON_MUXED OUT						
V_{OL}	LOW level output current	I_{OL} = 100 µA	—	—	0.4	V
V_{OL}	LOW-level output current	I_{OL} = 4 mA	—	—	0.7	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$	—	—	100	µA
GPIO						
V_{OL}	LOW-level output current	I_{OL} = 100 µA	—	—	0.4	V
V_{OL}	LOW-level output current	I_{OL} = 4 mA	—	—	0.7	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$	—	—	100	µA

NOTE:
1. V_{HYS} is the hysteresis of Schmitt-Trigger inputs

NON-VOLATILE STORAGE SPECIFICATIONS

PARAMETER	SPECIFICATION
Memory cell data retention	10 years min
Number of memory cell write cycles	100,000 cycles min

Application Note *AN250 I²C DIP Switch* provides additional information on memory cell data retention and the minimum number of write cycles.

AC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
MUX_INx ⇒ MUX_OUTx					
t_{PLH}	LOW-to-HIGH transition time	—	21	28	ns
t_{PHL}	HIGH-to-LOW transition time	—	7	10	ns
MUX_SELECT ⇒ MUX_OUTx					
t_{PLH}	LOW-to-HIGH transition time	—	20	28	ns
t_{PHL}	HIGH-to-LOW transition time	—	8	12	ns
$\overline{\text{MUX\_OUT\_LOW}}$ ⇒ NON_MUXED_OUT					
t_{PLH}	LOW-to-HIGH transition time	—	20	26	ns
t_{PHL}	HIGH-to-LOW transition time	—	8	15	ns
$\overline{\text{MUX\_OUT\_LOW}}$ ⇒ MUX_OUTx					
t_{PLH}	LOW-to-HIGH transition time	—	20	28	ns
t_{PHL}	HIGH-to-LOW transition time	—	7.0	15	ns
t_R	Output rise time	1.0	—	10	ns/V
t_F	Output fall time	1.0	—	5	ns/V
C_L	Test load capacitance on outputs	—	—	—	pF
I²C-bus					
t_{SCL}	SCL clock frequency	10	—	400	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3	—	—	µs
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	600	—	—	ns
t_{LOW}	LOW period of SCL clock	1.3	—	—	µs
t_{HIGH}	HIGH period of SCL clock	600	—	-12	ns
$t_{SU:STA}$	Set-up time for a repeated START condition	600	—	-32	ns
$t_{HD:DAT}$	Data hold time	0	—	10	ns
$t_{SU:DAT}$	Data set-up time	100	—	-100	ns
t_{SP}	Data spike time	0	—	50	ns
$t_{SU:STO}$	Set-up time for STOP condition	600	—	10	ns
t_R	Rise time for both SDA and SCL signals (10 - 400 pF bus)	20	—	300	ns
t_I	Fall time for both SDA and SCL signals (10 - 400 pF bus)	20	—	300	ns
C_L	Capacitive load for each bus line	—	—	400	pF
T_W	Write cycle time[1]	—	15	—	ms

NOTE:
1. WRITE CYCLE time can only be measured indirectly during the write cycle. During this time, the device will not acknowledge its I²C Address.

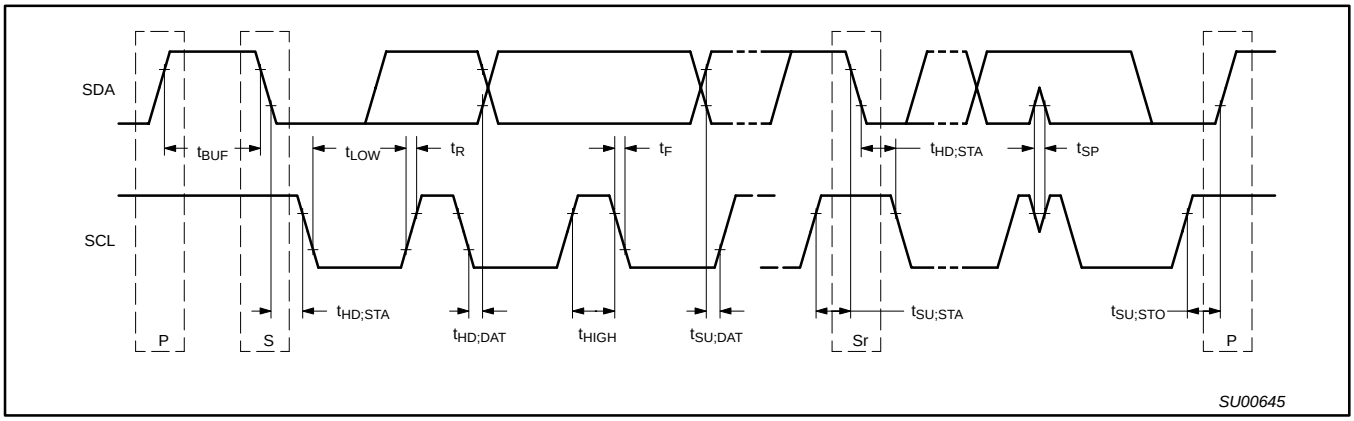


Figure 19. Definition of timing

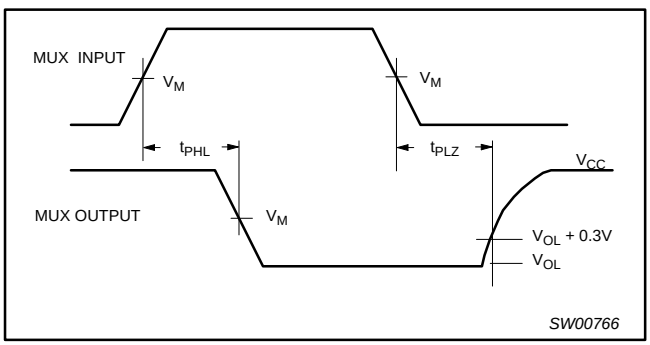


Figure 20. Open drain output enable and disable times

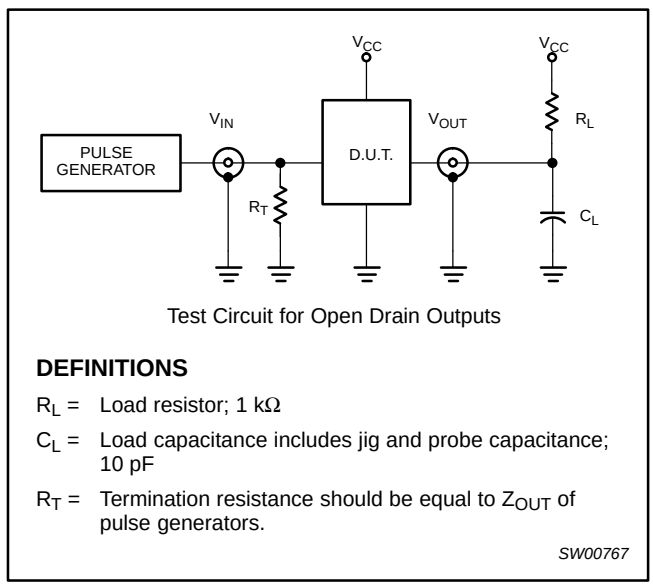
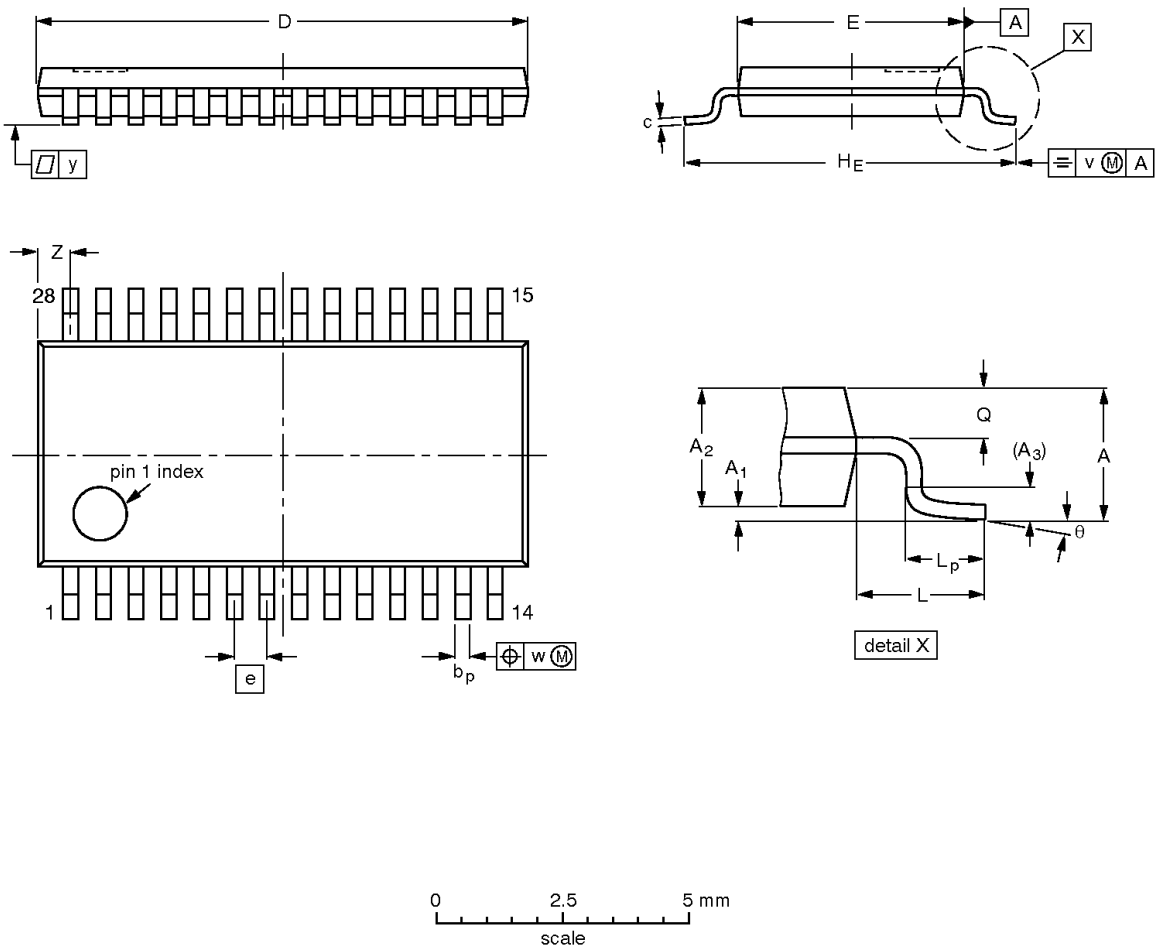


Figure 21. Test circuit

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm SOT361-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20030627	**Product data (9397 750 11674); ECN 853-2235 29936 dated 19 May 2003. Supersedes data of 2002 May 24 (9397 750 09889).** Modifications: • Update marketing information. • Increase number of write cycles from 3K to 100K.
_2	20020524	Product data (9397 750 09889); ECN 853-2235 28310 of 24 May 2002.

8-bit I²C and SMBus I/O port with 5-bit multiplexed/1-bit latched 6-bit I²C EEPROM DIP switch and 2-kbit EEPROM

PCA9558

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

Date of release: 06-03

Document order number: 9397 750 11674

Let's make things better.

Philips Semiconductors

PHILIPS